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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/545,785	04/07/2000	Tirdad Sowlati	US 000099	2253

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PHILIPS ELECTRONICS NORTH AMERICAN CORP  
580 WHITE PLAINS RD  
TARRYTOWN, NY 10591

EXAMINER

NADAV, ORI

ART UNIT	PAPER NUMBER
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2811

DATE MAILED: 05/20/2003

22

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/545,785

Applicant(s)

SOWLATI ET AL.

Examiner

ori nadav

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 21 April 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 07 April 2000 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

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## **DETAILED ACTION**

### ***Drawings***

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Figure 2B depicts dielectric layer comprising vacuum. Therefore, a silicon oxide dielectric layer must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.
2. The drawings are objected to because figure 2C should be corrected as previously corrected figure 2B. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

### ***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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4. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ng et al. (5,583,359) for reasons of record, as recited in previous office action (paper 10). Regarding claims 1 and 7, Ng et al. teach in figure 8 and related text a capacitor 200 over a substrate 202 comprising a first level 210 of at least four electrically conductive parallel lines extending in a first direction and lying in a first plane, at least a second level 212 comprising metal or polysilicon (column 9, lines 65-66) of at least four electrically conductive parallel lines extending in the first direction and lying in a second plane above the first plane, each of the second level lines being disposed over a respective one of the first level lines, such that the lines of the first and second levels are arranged in a series of at least four coplanar line pairs, each line pair comprising one of the first level lines and a respective one of the second level lines; a dielectric layer 250 (figure 9) disposed between the first and second levels of conductive lines; a plurality of vias 230 arranged in a plurality of groups corresponding uniquely to one of the coplanar line pairs and including at least two vias connecting the first level line and the second level line of the corresponding line pair (6 vias are depicted in figure 8), and electrically opposing nodes forming the terminals of the capacitor, the array of parallel capacitor plates electrically connected to the opposing nodes in an alternating manner so that the plates have alternating electrical polarities (figures 10-11).

Figure 8 does not depict an array of at least four parallel capacitor plates. Figure 10 depicts a capacitor comprises plurality of parallel capacitor plates (fingers) of alternating polarity. It would have been obvious to a person of ordinary skill in the art at the time

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the invention was made to use an array of at least four parallel capacitor plates in Ng et al.'s device, in order to adjust the capacitance of the device according to the requirements of the application in hand.

Regarding claim 4, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a dielectric layer comprising silicon dioxide in Ng et al.'s device, because silicon dioxide is a conventional dielectric material, of which judicial notice may be taken.

Regarding claims 5, 6, 14 and 19, Ng et al. teach in figure 8 at least a third level 214 of at least four electrically conductive parallel lines extending in the first direction and lying in a third plane above the first and second planes such that each of the third level lines is coplanar with a respective one of the line pairs, and a second dielectric layer 252 (figure 9) disposed between the second and third levels of conductive lines so that the third level of lines vertically extends the array of at least four parallel capacitor plates.

Regarding claims 8-11, Ng et al. teach a capacitor being formed using known CMOS techniques (column 2, lines 56-57). Therefore, the capacitor comprises a sub-micron CMOS structure, as claimed.

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Regarding claims 12 and 15, Ng et al. teach in figure 8 a plurality of vias 230 arranged opposite a next respective plurality of vias, with identical spacing of vias in each plurality of vias.

Regarding claims 13 and 18, Ng et al. teach in figure 8 a plurality of vias 230 directly connecting the first level line and the second level line of corresponding line pair.

Regarding claims 16 and 20, Ng et al. teach in figure 8 each group includes four vias.

Regarding claim 17, Ng et al. teach in figure 8 first and second vias connecting the first level line and the second level line of corresponding line pair at respective first and second ends of the first and second level lines, respectively, wherein the second ends are opposite the first ends along the first direction.

### ***Response to Arguments***

5. Applicant argues that the objection to figure 2B should be withdrawn, because figure 8 of Ng et al. also does not depict interlayer dielectric layers.

If applicant chooses not to depict interlayer dielectric layers in figure 2B of the present invention, the brief description of the drawings should state that figure 2B does not depict the interlayer dielectric layers.

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6. Applicant argues that figure 11 of Ng et al. depict that the first level line lacks sufficient number of vias, and vias 230 do not include any group corresponding uniquely to one of the coplanar line pairs.

Figure 8 of Ng et al. clearly depicts a first level line and a second level line being connected by at least 6 vias 230. Furthermore, any number of vias can chosen as being arranged in a group, and the group can correspond to any one of the coplanar line pairs. Therefore, Ng. et al. teach a plurality of vias 230 arranged in a plurality of groups corresponding uniquely to one of the coplanar line pairs and including at least two vias connecting the first level line and the second level line of the corresponding line pair (6 vias are depicted in figure 8), as claimed.

**Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.**

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Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(703) 308-8138**. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached at **(703) 308-2772**.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**



O.N.  
May 19, 2003

ORI NADAV  
PATENT EXAMINER  
TECHNOLOGY CENTER 2800